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a latch which, in response to one of said plurality of control signals, controllably provides said data output by said deserializer to said receive memory device;

each of said transmit [datapath] datapaths including a serializer configured to receive parallel data and output serial data.

Remarks

In view of the foregoing amendments and following remarks responsive to the Office Action of November 15, 1995, Applicants respectfully request favorable reconsideration of this application.

In section 1 of the Office Action, the Examiner rejected claims 1-13 under 35 U.S.C. § 112, second paragraph, as being indefinite. Particularly, the Examiner stated that, in claim 1, "said memory means" lacks clear antecedent basis because line 6 defines a receive memory and a transmit memory. Applicant has amended claim 1 to recite "said receive memory means" in order to overcome this rejection.

The Examiner also stated that "said transmit datapath" in claim 1 lacks clear antecedent basis because line 12 states that each data station corresponds to a transmit datapath. The Examiner asked if "each" should be inserted before "said transmit."

The Examiner's position is well taken and Applicants have herein inserted "each" as suggested.

In section 3 of the Office Action, the Examiner rejected claim 14 under 35 U.S.C. § 103 as being unpatentable over Sakurai. In particular, the Examiner asserted that Sakurai teaches receive and

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transmit datapaths, the receive datapath including a serial-to-parallel converter 27, and a latch circuit 28 for latching the data from the serial-to-parallel converter 27 in response to a control signal from the detection circuit 20. The Examiner further asserted that the transmit datapath has a parallel-to-serial converter 24.

The Examiner noted that Sakurai does not explicitly recite a receive memory and a transmit memory. However, the Examiner further referred to prior art figure 10 of Sakurai which describes a conventional communication system in which the communication station comprises a receiving buffer 9 and a transmitting buffer 11 connected to a CPU 10. The Examiner asserted that it would have been obvious to provide the receive datapath and the transmit datapath in the device shown in figure 1 with the receive and transmit buffers taught in the conventional system of figure 10 because data received from the medium must be stored for further processing by the processor, and transmit data must be temporary stored to avoid data loss if the medium is not available.

Applicants respectfully traverse this rejection. The purpose of the latch (1314 in Figure 13) which is recited in claim 14 is explained on page 23, lines 30-34 of the application as follows:

> Data loading into the RX-buffer 132 is 10 bits parallel, i.e., from one physical layer port per cycle. Since a new slot of data comes in every 10 clock cycles and there are 16 data bytes to be loaded, an additional stage of buffers 1314 (rx_latch) in the receive datapath is provided.

In other words, the series of latches in the RX datapaths in the present invention are to handle data

contentions between the various parallel receive datapaths.

Sakurai contains no corresponding teaching. Accordingly, not only is the asserted combination not suggested by the prior art, but it is actually taught away from by Sakurai and would not make any sense in Sakurai in any event. Particularly, the circuit shown in Figure 1 is intended to be a wholesale replacement of the conventional circuit shown in Figure 11. Accordingly, combining pieces of the two different circuits not only is not suggested in the prior art, but doesn't make sense. The two circuits perform basically the same function. One would not simply add another buffer into the circuit of Figure 1, since there is no apparent reason for doing so in Sakurai, let alone placing it in the particular location dictated by claim 14.

In any event, in the Sakurai circuit, there is only one "receive" datapath to parallel output k. That path is through output latch circuit 28. The purpose of latch 28 apparently is to prevent the output of the continuously operating serial-to-parallel converter 27 from getting to the output k latch unless an address coincidence is detected. It has nothing to do with data contentions with other datapaths into parallel output k since there are no other datapaths into parallel output k.

Accordingly, Sakurai does not teach "a receive memory device and a transmit memory device" as recited in claim 14.

Nevertheless, Applicant has amended claim 14 to even more clearly distinguish over Sakurai. Particularly, claim 14 did not previously recite that there is a plurality of parallel receive and transmit datapaths. Applicant has now amended claim 14 to expressly recite this limitation, thus providing an even clearer distinction over Sakurai.

In view of the foregoing amendments and remarks, this application is now in condition for allowance. Applicant respectfully requests the Examiner to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

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